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Carrier Distortion in Hysteretic Self-Oscillating Class-D Audio Power Amplifiers: Analysis and Optimization

Mikkel C. W. Høyerby, *Member, IEEE*, and Michael A. E. Andersen, *Member, IEEE*

***Abstract*—An important distortion mechanism in hysteretic self-oscillating (SO) class-D (switch mode) power amplifiers—carrier distortion—is analyzed and an optimization method is proposed. This mechanism is an issue in any power amplifier application where a high degree of proportionality between input and output is required, such as in audio power amplifiers or xDSL drivers. From an average-mode point of view, carrier distortion is shown to be caused by nonlinear variation of the hysteretic comparator input average voltage with the output average voltage. This easily causes total harmonic distortion figures in excess of 0.1–0.2%, inadequate for high-quality audio applications. Carrier distortion is shown to be minimized when the feedback system is designed to provide a triangular carrier (sliding) signal at the input of a hysteretic comparator. The proposed optimization method is experimentally proven in an audio power amplifier leading to THD figures that are comparable to the state of the art. Experimental hardware is a hysteretic SO bandpass current-mode-controlled single-ended audio power amplifier capable of 45 W into 8 Ω or 80 W into 4 Ω from a ±34 V supply with less than 0.03% THD from 100 Hz to 6.7 kHz. Carrier distortion is shown to account for this limitation in THD performance.**

***Index Terms*—Audio, class-D, hysteretic, power amplifier, sliding.**

I. Introduction

SWITCH-MODE (class D) audio power amplifiers have been a commercial success over the past decade, replacing traditional linear (class A/AB/B) amplifiers in many applications. The main driver has been the reduction in physical size resulting from the increased efficiency [1].

It is generally well understood that errors in the switching stage of the class-D amplifier can introduce significant harmonic distortion to the amplifier output [1]–[3]. However, with the ever-increasing performance of modern power MOSFETs, the significance of switching stage errors diminishes [4], [5]. As a result, the distortion generated by the pulsewidth modulation (PWM) and control process itself becomes visible. An excellent illustration of this is given in [5], where the distortion generated by the injection of switching ripple components from the feedback circuitry into the PWM is analyzed by the use of discrete-time system theory. As presented, this analysis is only applicable to clocked/driven control systems, such as those based on the traditional triangle-and-comparator PWM.

For self-oscillating (SO) control systems, which have been successfully commercialized [6] for class-D audio, details on the distortion generated by the modulation and control process are more scarce, although a very good example is given in [7] for SO systems without comparator hysteresis. However, design suggestions on how to affect the amount of distortion generated by the modulation process are not offered, nor does the analysis directly apply to SO systems with comparator hysteresis. For these systems, only a few hints on optimizing modulation linearity are offered [8]–[10].

This paper examines distortion generated by the modulation process in the hysteretic SO class of control systems, a class that has yielded some of the most impressive [9], [11] THD figures published for switch-mode audio power amplifiers. The analysis is carried out using the well-established average modeling approach, leading to an optimization method proposal that is consistent with prior art findings, and complemented by experimental results on a representative, nontrivial, hysteretic SO class-D audio power amplifier. Although this paper is focused on audio power amplification, other applications exist where accurate amplification of ac signals is required. One example is various digital subscriber line (xDSL) drivers [7], where high output spectral purity is required. Another example is tracking power supplies in high-efficiency RF power amplification systems [12]. Here, the tracking power supply in some schemes directly modulates the output of an RF power amplifier, adding any distortion introduced by the tracking power supply to the RF power amplifier output. A final example is ac transmission systems [13], [14].

II. Hysteresis-Based SO Controllers

The hysteresis-based SO controllers reviewed in this paper can be considered a small, low-complexity subset of the very large set of sliding-mode control (SMC) systems. For audio power amplification using a single-phase buck-type power stage, the hysteretic SO control system will generally contain one comparator with hysteresis, which, based on a linear combination of system states and the audio input, selects one of the two possible switching states (high/low) for the power stage.

A very simple but applicable example of such a control system is the astable integrating multivibrator (AIM) [8], [15] shown in Fig. 1. Capable of good results [8] in practice, it has the

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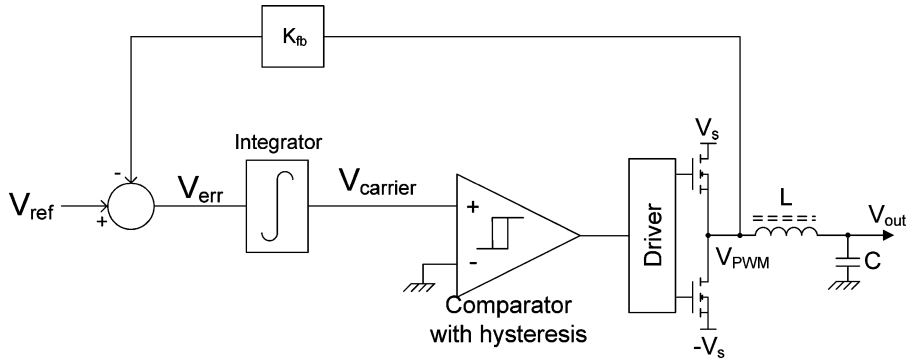

Fig. 1. Simple hysteretic SO audio power amplifier example—the AIM [8], [15].

disadvantage of not having feedback around the output filter, increasing the impact of the output filter design on amplifier distortion levels, output impedance, and frequency response [6], [9], [11]. Several alternative hysteretic SO controller implementations have been proposed in the context of audio power amplification, where the main difference lies in the way in which the output inductor current is effectively fed back, since this is the most difficult system state to measure. Some solutions opt for feeding back the output capacitor current instead, since this is the same as the inductor current with output current feedforward added [16]. The capacitor current can either be estimated by differentiation of the capacitor voltage [9], [17] and added to the raw capacitor voltage as done by proportional-derivative (PD) feedback, or measured directly with a current sense transformer [11], [18]. Alternatively, the inductor current can be estimated by low-pass filtering of the inductor voltage [10], effectively leading to bandpass current control [19]. In all cases, the use of postfilter feedback generally serves to lessen the negative effects of the output filter. Many very similar solutions have appeared in the somewhat wider context of single-phase buck dc/dc converters, where PD-based capacitor voltage feedback is richly represented [20]–[23] along with capacitor current feedback [24], [25] and direct inductor current feedback [26]. It has also been shown that the equivalent series resistance of the output capacitor can be usefully incorporated into the capacitor current estimation system [27], relaxing the demands on the differentiation circuitry.

At this time, it is useful to formally define the class of systems studied as any system with a hysteretic comparator driving a linear time-invariant system with relevant feedback and reference inputs added, as shown in Fig. 2. Of particular interest, it turns out, is the generation of the carrier signal ($V_{\rm carrier}$), which is described by the effective controller transfer function (a.k.a. "loop filter" [5]), $G_{\rm ctrl}(s)$:

$$G_{\rm ctrl}(s) \equiv \frac{V_{\rm carrier}(s)}{V_{\rm PWM}(s)} \tag{1}$$

These generalizations allow all of the aforementioned systems to be represented, and are often adopted in prior art [28]–[30].

As sliding mode controllers, extensive theory [31] exists for dealing with the stability and dynamics of hysteretic SO controllers. In the application of controlling simple switch-mode power converters, classical sliding mode theory is based on the assumption

$$V_{\rm carrier} = 0 \tag{2}$$

where $V_{\rm carrier}$ is the input to the hysteretic comparator, generally known as the "sliding variable" in SMC context or the "carrier signal" in SO control context. This approximation can be very useful [32], but also has its shortcomings [16]. For the presented study of linearity and distortion in sliding mode controllers, it is absolutely essential to depart from this basic assumption. The carrier voltage is still usefully described as *almost* zero, but the implications of "almost" need to be considered

$$V_{\rm carrier} \approx 0 \tag{3}$$

Prior art has demonstrated several examples of this; a nonzero carrier average was used in [33] to assign a low-frequency gain to the hysteretic comparator, and it is well known [34] that a describing function can be used to find its gain at the switching/oscillation frequency of the control loop. These two methods can even be combined to yield an estimated, but still quite accurate, transfer function for the hysteretic comparator [35]. A nonzero carrier average caused by delays in the comparator and power stage is shown in [36] to lead to inaccuracy in the average output current of a hysteretic current control loop. In the following, the effects of nonzero carrier average caused by the properties of $G_{\rm ctrl}(s)$ are examined.

III. Carrier Distortion

The carrier distortion [8] mechanism in hysteretic SO controllers is claimed [8]–[10] to be a function of the shape of the carrier signal waveform, with a triangular waveform being the optimum. In order to properly explain this proposed distortion mechanism, it is useful to examine the simplest conceivable hysteretic SO control system: the AIM. The approach adopted is to analyze the average (dc) carrier voltage variation with the amplifier dc operating point, expressed as a steady-state duty cycle D for different degrees of integrator ideality. Under the assumption of quasi-stationary behavior, the dc characteristics of the loop will also apply at audio frequencies [5]. Practically, the integrator in the AIM is replaced with a pole and a gain to provide variable carrier signal "straightness" in a way that is simple enough to allow exact analysis. With this imperfect

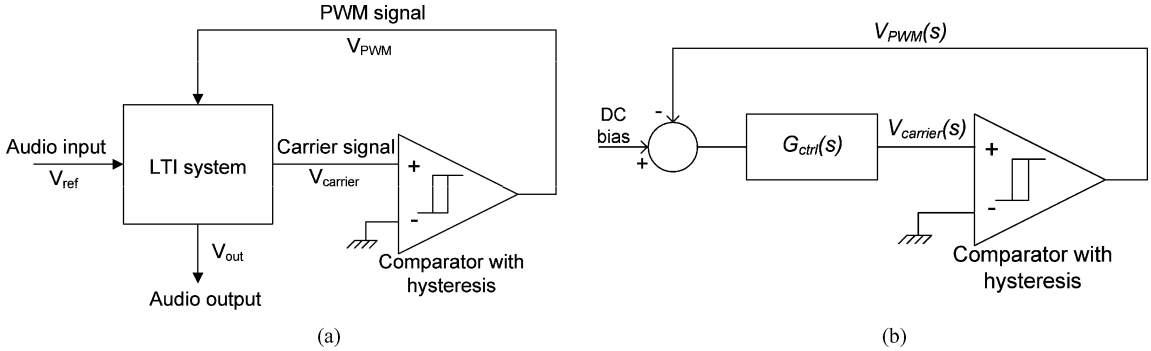

Fig. 2. Generalized views of hysteretic SO control systems for audio applications. (a) Overall system. (b) Carrier generation process.

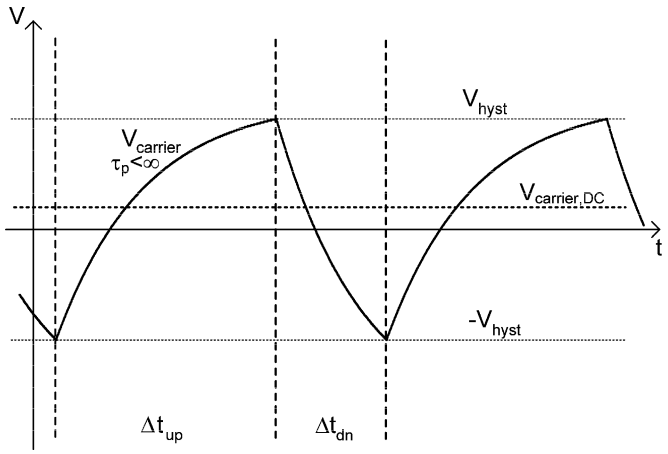

Fig. 3. AIM carrier waveform ($D = 1/3$) with single-pole $G_{\mathrm{ctrl}}(s)$ as considered for carrier distortion analysis. $V_{\mathrm{carrier,dc}}$ is the average of the carrier waveform, which evidently can be nonzero in spite of a symmetrical hysteresis window $\pm V_{\mathrm{hyst}}$ and zero delay.

integrator, a representative example of the carrier signal in the AIM is shown in Fig. 3. Note that zero time delay in the comparator and power stage has been assumed for the analysis performed hereafter. $\pm V_{\mathrm{hyst}}$ denotes the hysteresis window. Likewise, it has been assumed that $V_s = 1$ and $K_{fb} = 1$ in order to clarify the analysis.

The AIM loop integrator is replaced with the transfer function $G(s)$, which also becomes the $G_{\mathrm{ctrl}}(s)$ of the system

$$G(s) = G_{\mathrm{ctrl}}(s) = \frac{G_p}{1 + s\tau_p} \tag{4}$$

Note that G_p is a gain that numerically equals τ_p, a distinction made to avoid unit confusion in the following analysis. The purpose of this particular choice of G_p is to ensure that $G_{\mathrm{ctrl}}(s)$ converges toward the ideal integrator when τ_p is made large

$$\lim_{\tau_p \to \infty} G_{\mathrm{ctrl}}(s) = \frac{1}{s} \tag{5}$$

The step response of $G_{\mathrm{ctrl}}(s)$ is given by

$$\mathrm{step}\{G_{\mathrm{ctrl}}(s)\} = G_p(1 - e^{-(t/\tau_p)}) \tag{6}$$

Assuming that the feedback system has high loop gain, the steady-state PWM voltage per-cycle average will represent the reference voltage exactly

$$\langle V_{\mathrm{PWM}} \rangle_{T_{\mathrm{sw}}} = V_{\mathrm{ref}} \tag{7}$$

This allows the reference voltage to be expressed by the PWM signal steady-state duty cycle D

$$\langle V_{\mathrm{PWM}} \rangle_{T_{\mathrm{sw}}} = 2(D-1) \Rightarrow V_{\mathrm{ref}} = 2(D-1) \tag{8}$$

The input to the loop filter is given by

$$V_{\mathrm{err}} = V_{\mathrm{ref}} - V_{\mathrm{PWM}} = \begin{cases} V_{\mathrm{ref}} + 1, & V_{\mathrm{PWM}} = -1 \\ V_{\mathrm{ref}} - 1, & V_{\mathrm{PWM}} = 1 \end{cases} \tag{9}$$

This can be rewritten as

$$V_{\mathrm{err}} = \begin{cases} 2D, & V_{\mathrm{PWM}} = -1 \\ 2(D-1), & V_{\mathrm{PWM}} = 1 \end{cases} \tag{10}$$

In this case, D and $(D-1)$ both stringently have the unit of V. Since the PWM signal can be considered as a series of step functions, a segment of the carrier voltage can be found by using the step response of $G_{\mathrm{ctrl}}(s)$ and observing that an initial value has to be added to reflect the presence of the hysteresis window $\pm V_{\mathrm{hyst}}$. The carrier voltage will change exponentially with time constant τ_p and initial and final values as given in Table I.

TABLE I
CARRIER SIGNAL INITIAL/FINAL CONDITIONS IN AIM WITH IMPERFECT INTEGRATOR

PWM level	Initial (t=0) value	Final (t=∞) value
$V_{PWM} = -1$	$-V_{hyst}$	$2 \cdot D \cdot G_p$
$V_{PWM} = 1$	V_{hyst}	$2 \cdot (D-1) \cdot G_p$

The carrier voltage can thus be described as

$$V_{\mathrm{carrier}}(t) = \begin{cases} -V_{\mathrm{hyst}} + (2DG_p + V_{\mathrm{hyst}})\left(1 - e^{-(t/\tau_p)}\right), & V_{\mathrm{PWM}} = -1 \\ V_{\mathrm{hyst}} + (2(D-1)G_p - V_{\mathrm{hyst}})\left(1 - e^{-(t/\tau_p)}\right), & V_{\mathrm{PWM}} = 1 \end{cases} \tag{11}$$

The up/down-slope periods Δt_{up} and Δt_{dn} can now be found by adding the boundary condition of the carrier signal hitting the hysteresis window, leading to the equations

$$\begin{aligned} &-V_{\mathrm{hyst}} + (2DG_p + V_{\mathrm{hyst}})\left(1 - e^{-(\Delta t_{\mathrm{up}}/\tau_p)}\right) = V_{\mathrm{hyst}} \wedge V_{\mathrm{hyst}} \\ &+ (2(D-1)G_p - V_{\mathrm{hyst}})\left(1 - e^{-(\Delta t_{\mathrm{dn}}/\tau_p)}\right) = -V_{\mathrm{hyst}} \end{aligned} \tag{12}$$

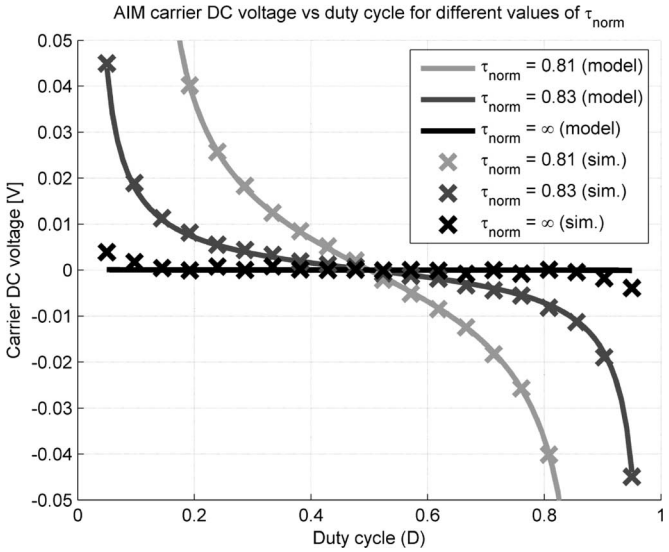

Fig. 4. Modeled (16) and simulated carrier dc voltages plotted for variable duty cycle. Modeled results match simulated results very well.

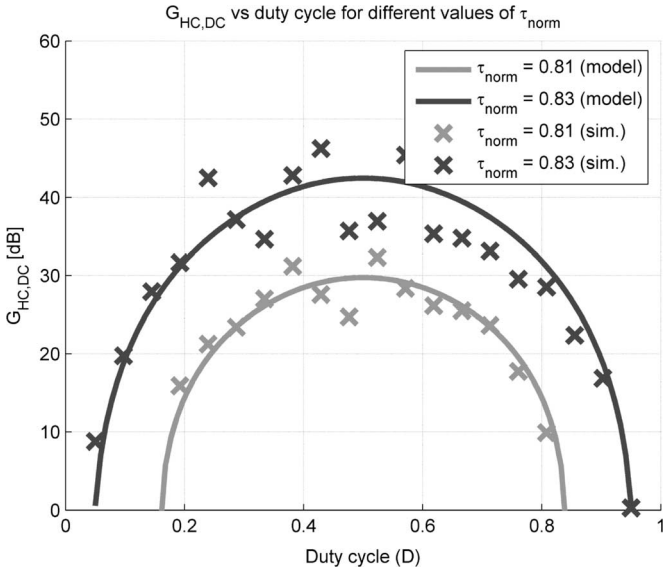

Fig. 5. Modeled [using numerical evaluation of (17)] and simulated hysteretic comparator dc gain $G_{\mathrm{HC,dc}}$. Deviation from the ideal loop filter ($\tau_p = \infty$) causes reduction and nonlinearity in $G_{\mathrm{HC,dc}}$. Results for $\tau_p = \infty$ would be a horizontal line at $G_{\mathrm{HC,dc}} = \infty$. The nonlinearity is symmetrical around $D = 0.5$, so only odd harmonic distortion is produced.

These equations can be solved easily, leading to

$$\begin{aligned}\Delta t_{\mathrm{up}} &= -\tau_p \ln\left(1 - \frac{2V_{\mathrm{hyst}}}{2DG_p + V_{\mathrm{hyst}}}\right) \wedge \Delta t_{\mathrm{dn}} \\ &= -\tau_p \ln\left(1 - \frac{2V_{\mathrm{hyst}}}{2\left(1-D\right)G_p + V_{\mathrm{hyst}}}\right) \end{aligned} \tag{13}$$

In order to provide a more general view of the influence of τ_p on system behavior, τ_p can be normalized to the nominal ($D = 0.5$) switching period ($T_{\mathrm{sw,nom}}$) of the loop

$$\tau_{\mathrm{norm}} = \frac{\tau_p}{T_{\mathrm{sw,nom}}} = \left.\frac{\tau_p}{\Delta t_{\mathrm{up}} + \Delta t_{\mathrm{dn}}}\right|_{D=0.5} \tag{14}$$

Now, the only problem is to find the average (dc) value of the carrier voltage with the given variables. This is done by calculating the per-cycle average of the carrier by integrating the carrier voltage over one switching period

$$V_{\mathrm{carrier,dc}}\left(D\right) = \frac{1}{\Delta t_{\mathrm{up}} + \Delta t_{\mathrm{dn}}} \int_0^{\Delta t_{\mathrm{up}} + \Delta t_{\mathrm{dn}}} V_{\mathrm{carrier}}\left(t\right)\, dt \tag{15}$$

Solving this integral (Mathematica was used for symbolic solution) results in (16) as shown at the bottom of this page.

This expression is best analyzed by plotting the expression output for different parameter inputs as in Fig. 4. It is obvious that the carrier dc voltage varies with D in a nonlinear manner when the loop filter is not an integrator. If τ_p approaches infinity, this expression can be shown to converge toward zero. Since the gain of the hysteretic comparator can be defined as

$$\begin{aligned} G_{\mathrm{HC,dc}}\left(D\right) &\equiv \frac{\left(\partial \left\langle V_{\mathrm{PWM}}\right\rangle_{T_{\mathrm{sw}}}\right)/\partial D)}{\left(\partial V_{\mathrm{carrier,dc}}\left(D\right)\right)/\partial D)} \\ &= \frac{2}{\left(\partial V_{\mathrm{carrier,dc}}\left(D\right)\right)/\partial D)} \end{aligned} \tag{17}$$

it is also obvious that the hysteretic comparator exhibits a nonconstant gain at dc. In other words, a nonlinear element has been introduced into the loop, leading to harmonic distortion. This distortion generated by the nonlinear variation of $V_{\mathrm{carrier,dc}}$ with D is exactly what has previously been named *carrier distortion.*

For the AIM with the considered, imperfect loop filter, even with all the simplifications made (zero time delay, only dc considered), the analytical expression for $G_{\mathrm{HC,dc}}$ gets too complicated to be of real value, so numerical differentiation was used for finding the carrier dc voltage derivative. Analytical and simulated values of $G_{\mathrm{HC,dc}}$ are shown in Fig. 5. Since $V_{\mathrm{carrier,dc}}(D)$ is generally larger and more variable for smaller values of τ_{norm}, the dc gain of the hysteretic comparator also decreases with τ_{norm}. Since the average of a perfectly triangular carrier oscillating within $\pm V_{\mathrm{hyst}}$ is zero, the dc gain of the hysteretic comparator could theoretically be infinite. In practice, time delay in the comparator (and power stage) ensures that this never happens [33], [35].

In order to evaluate the effect of the found variation of $V_{\mathrm{carrier,dc}}$ with D on amplifier distortion, the system is modeled as shown in Fig. 6.

$$V_{\mathrm{carrier,dc}}\left(D\right) = -2G_p \frac{\left(1-D\right)\ln\left(1 - \left(2V_{\mathrm{hyst}}/\left(2G_p\left(1-D\right) + V_{\mathrm{hyst}}\right)\right)\right) - D\ln\left(1 - \left(2V_{\mathrm{hyst}}/\left(2G_pD + V_{\mathrm{hyst}}\right)\right)\right)}{\ln\left(1 - \left(2V_{\mathrm{hyst}}/\left(2G_p\left(1-D\right) + V_{\mathrm{hyst}}\right)\right)\right) + \ln\left(1 - \left(2V_{\mathrm{hyst}}/\left(2G_pD + V_{\mathrm{hyst}}\right)\right)\right)} \tag{16}$$

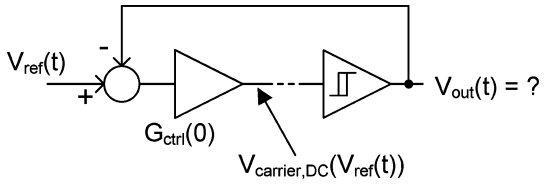

Fig. 6. Model of the AIM loop used for determination of output voltage waveform when taking carrier distortion into consideration. Reference signal $V_{\mathrm{ref}}(t)$ is assumed to be dc or "almost dc."

The output of the AIM model in Fig. 6 is given by

$$V_{\mathrm{out}}(t) = V_{\mathrm{ref}}(t) - \frac{V_{\mathrm{carrier,dc}}(V_{\mathrm{ref}}(t))}{G_{\mathrm{ctrl}}(0)} \tag{18}$$

The output, V_{out} is here formally defined as the per-(switch)-cycle average PWM voltage

$$V_{\mathrm{out}} \equiv \langle V_{\mathrm{PWM}} \rangle_{T_{\mathrm{sw}}} \tag{19}$$

Assuming that the output voltage has relatively low distortion, the D of the AIM will be determined almost exclusively by V_{ref}. Thus, for a given V_{ref}, D is approximated as

$$D = \frac{1}{2}(V_{\mathrm{ref}} + 1) \tag{20}$$

For a sinusoidal input

$$V_{\mathrm{ref}}(t) = M \sin(2\pi f_{\mathrm{ref}} t) \tag{21}$$

the duty cycle is therefore approximated as

$$D(t) = \frac{1}{2}[M \sin(2\pi f_{\mathrm{ref}} t) + 1] \tag{22}$$

Note that since the studied AIM has a reference-to-output gain of unity and conceptually operates from 1 V supplies, the amplitude M of the sine wave corresponds to the modulation index of the PWM signal. The peak duty cycle $D_{\max}$ and the modulation index M are generally related as follows:

$$D_{\max} = \frac{1}{2}(1 + M) \tag{23}$$

Thus, the output of the AIM is

$$V_{\mathrm{out}}(t) = \frac{1}{2}[M \sin(2\pi f_{\mathrm{ref}} t) + 1] - \frac{V_{\mathrm{carrier,dc}}\left(\frac{1}{2}[M \sin(2\pi f_{\mathrm{ref}} t) + 1]\right)}{G_{\mathrm{ctrl}}(0)} \tag{24}$$

This expression is best evaluated numerically, yielding the averaged output of the AIM, complete with carrier distortion. As shown in the calculated example waveforms in Fig. 7, the distortion generated by using a pole as a loop filter in the AIM is of expansive character, causing the peaks of the reference signal to come out at a higher level than desired. This is perhaps surprising, since $G_{\mathrm{HC,dc}}$ is reduced at high D. However, this compressive action is more than counteracted by the requirement for a specific carrier dc voltage $V_{\mathrm{carrier,dc}}$ to be present for a given D. As an example, assume that the reference is $+0.5$. The loop will attempt to establish a D of 0.75, but looking at Fig. 4, the carrier voltage must contain a small,

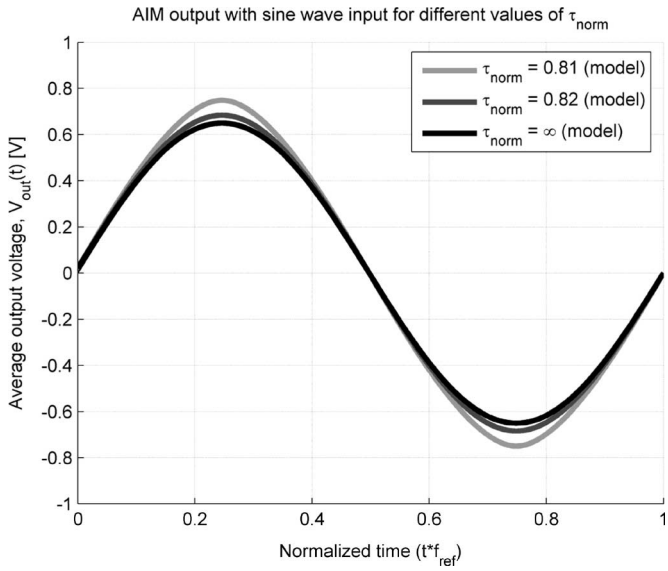

Fig. 7. Calculated AIM output with values of $\tau_{\mathrm{norm}}(M = 0.65)$. Carrier distortion caused by small time constants causes signal expansion at high output levels.

negative dc component. Looking at Fig. 6, this can only be produced by an output dc voltage that is slightly higher than prescribed by the reference, causing the expansion effect apparent in Fig. 7.

From the AIM output, harmonic distortion products are found by Fourier analysis. The output waveform is expressed by the Fourier series (with complex coefficients) given by

$$c_{\mathrm{out},n} = f_{\mathrm{ref}} \int_{t=0}^{t=(1/f_{\mathrm{ref}})} V_{\mathrm{out}}(t)\, e^{-j2\pi f_{\mathrm{ref}} n}\, dt \tag{25}$$

where $|c_{\mathrm{out},1},|$ corresponds to the fundamental amplitude, $|c_{\mathrm{out},3},|$ corresponds to the third-harmonic distortion product, etc. The THD generated by carrier distortion can be calculated from these numbers by evaluating the following expression:

$$\mathrm{THD} = \frac{\sqrt{|c_{\mathrm{out},2}|^2 + |c_{\mathrm{out},3}|^2 + \cdots + |c_{\mathrm{out},n}|^2}}{|c_{\mathrm{out},1}|} \tag{26}$$

In practice, the following expression is a good approximation since there are no even harmonics:

$$\mathrm{THD} \approx \frac{\sqrt{|c_{\mathrm{out},3}|^2 + |c_{\mathrm{out},5}|^2 + \cdots + |c_{\mathrm{out},n}|^2}}{|c_{\mathrm{out},1}|} \tag{27}$$

In the studied AIM example, we numerically evaluate harmonics and THD from the derived analytical expressions and compare them with simulations results in the numbers shown in Figs. 8–11. It is evident that the analysis approach shown is capable of describing the carrier distortion mechanism very well. It is also evident that this mechanism can easily produce significant harmonic distortion in an amplifier with a perfect power stage with stiff supply voltage, and no delay and no dead-time distortion, justifying the analysis performed. Finally, the generated distortion exhibits strong variation with τ_{norm} in the area of 0.80–0.85. This simply reflects that the first segment (well

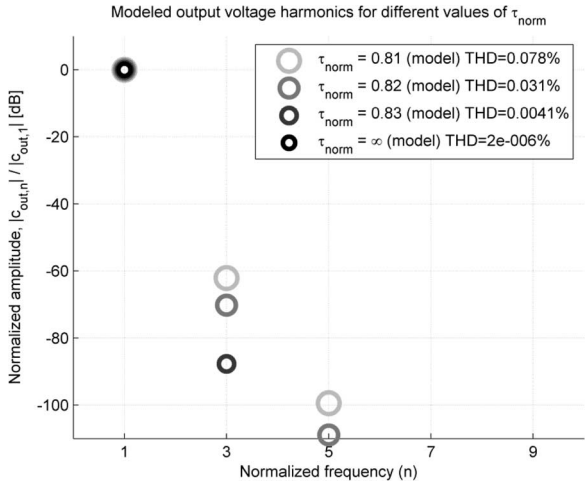

Fig. 8. Output harmonics from AIM found by calculation; $M = 0.2$.

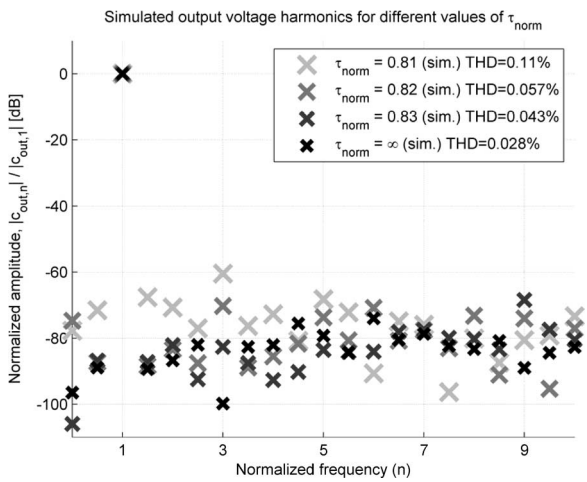

Fig. 9. Output harmonics from AIM found by simulation; $M = 0.2$.

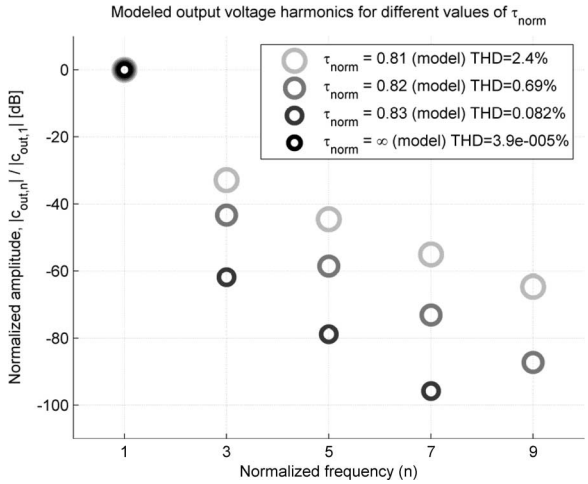

Fig. 10. Output harmonics from AIM found by calculation; $M = 0.65$.

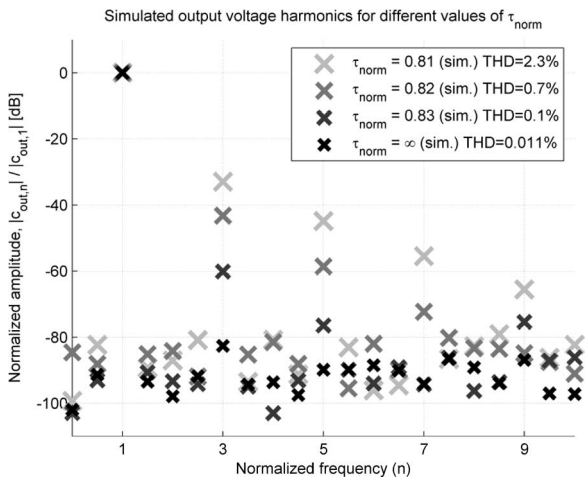

Fig. 11. Output harmonics from AIM found by simulation; $M = 0.65$.

below $t = \tau_p$) of an exponentially shaped carrier has almost-constant slope, with curvature becoming significantly closer to τ_p.

Several implications result from this analysis. First, it allows for proper explanation of the carrier distortion phenomenon by reference to the average modeling technique used. The explanation offered is that a nontriangular carrier signal (the result of not having an integrator-type $G_{\mathrm{ctrl}}(s)$) requires voltages that are a nonlinear function of the reference voltage to be present at the hysteretic comparator input, directly causing distortion, and in the process causing the hysteretic comparator to exhibit a nonconstant small-signal dc gain. Second, it allows the amount of carrier distortion in a class-D audio amplifier design to be predicted analytically from data on the carrier signal dc voltage. This is useful information in that it provides a designer with a tool for determining just how "perfect" the carrier signal should be to meet a target THD specification without time-consuming, repetitive simulations of multiple reference signal periods. Finally, the analysis supports statements in prior art [8] claiming that the carrier signal should be triangular (resulting from the use of an integrator as loop filter in the AIM), arguing from the point of view that the carrier voltage dc component should be a linear function of duty cycle to avoid causing nonlinearity. It is then taken as a trivial matter to show that a perfectly triangular carrier oscillating between $\pm/-V_{\mathrm{hyst}}$ has to have an average of zero for any D.

IV. Carrier Distortion Optimization

The previous section provided an analytical justification for pursuing a triangular carrier signal. In an AIM, this is easy; any practical operational amplifier has enough dc gain for realizing a loop filter that sufficiently resembles an integrator. In other feedback configurations, however, the problem is much more severe. For example, considering the hysteretic bandpass current-mode (BPCM) control topology demonstrated in [10] (and illustrated in Fig. 12), it is not obvious how to make the output of the combined voltage and current estimate feedbacks respond with a ramp to a step input, except perhaps by perfect estimation of the inductor current and removal of the output voltage feedback. This would make the amplifier a current source instead of the desired voltage source. The hysteretic BPCM topology has still been demonstrated to be capable of very good THD figures

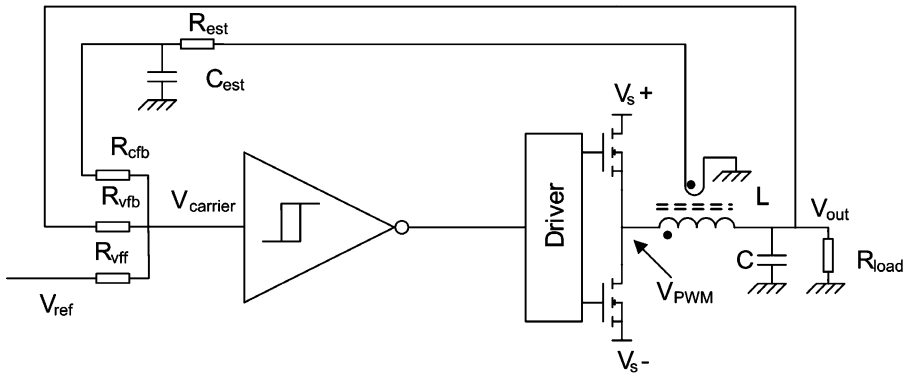

Fig. 12. Simple single-ended BPCM amplifier implementation [10].

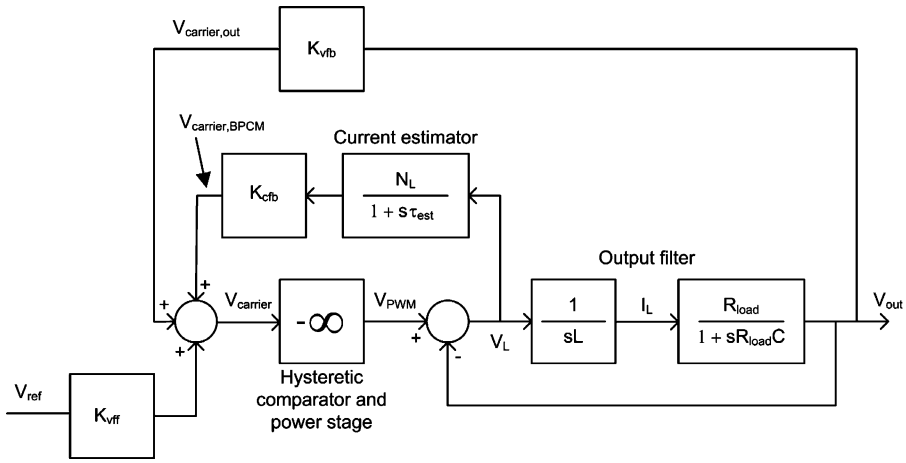

Fig. 13. Small-signal model of BPCM amplifier [10] using infinite-gain (equivalent to assuming sliding-mode operation [23], [31]) hysteretic comparator model.

(0.01%–0.03% range) with a modest control system complexity. It is a dual-loop feedback system, which incorporates the output filter dynamics, making the loop design nontrivial in comparison with the AIM. As such, it is an ideal test vehicle for the demonstration of a new analytical carrier distortion minimization technique based on the pursuit of a triangular carrier signal.

The carrier linearization approach that is proposed has the objective of shaping the step response of $G_{\rm ctrl}(s)$ as a ramp. The proposed method for minimization and evaluation of carrier distortion is simply as follows.

1) Compute the step response of $G_{\rm ctrl}(s)$ analytically.
2) Compute second (time-) derivative of $G_{\rm ctrl}(s)$ step response.
3) Use second derivative to find criteria for ensuring constant-sloping step response.
4) Use found criteria to design control loop.
5) Optional: fine-tune design by iterative simulations.
6) Optional: Evaluate $V_{\rm carrier,dc}(D)$ of design and determine carrier distortion-caused THD.

Step 3 is the main part of the method--since a constant-sloping (carrier) signal is characterized by its second derivative being zero, forcing the second derivative of the carrier signal response to a PWM step to be zero should lead to a constant-sloping (linear) carrier signal. Step 5 is typically the only tool available. It has been included since a number of approximations must be made when computing the step response of $G_{\rm ctrl}(s)$, resulting in a design that may be slightly suboptimal. Still, the proposed method saves considerable design time by reducing the number of iterative simulations required or removing these completely. Step 6 allows for a prediction of the minimum level of THD that can be expected from the optimized design, providing a second-source reference for comparison with simulated THD. The remaining parts of this section illustrate the proposed approach with the BPCM-controlled amplifier. Fig. 13 shows how the BPCM amplifier may be broken down to block diagram form, with relevant parameters summarized in Table II.

For the carrier generation, the contributions from two feedback paths (current estimate and output voltage) can be expressed by the following transfer functions:

$$G_{\rm BPCM}(s) \equiv \frac{V_{\rm carrier,BPCM}(s)}{V_{\rm PWM}(s)} = K_{\rm cfb} \times \frac{N_L}{1+s\tau_{\rm est}} \times \frac{1}{s^2LC + (L/R_{\rm load})s + 1} \times sL \times \frac{1+sR_{\rm load}C}{R_{\rm load}}$$

$$G_{\rm out}(s) \equiv \frac{V_{\rm carrier,out}(s)}{V_{\rm PWM}(s)} = K_{\rm vfb} \times \frac{1}{s^2LC + (L/R_{\rm load})s + 1} \quad (28)$$

TABLE II
PARAMETERS IN HYSTERETIC BPCM AMPLIFIER MODEL

Load resistance	R_{load}
Output filter capacitance	C
Output filter inductance	L
Inductor sense winding ratio	N_L
Current estimator time constant	τ_{est}
Current feedback coefficient	K_{cfb}
Voltage feedback coefficient	K_{vfb}
Reference feed-forward coefficient	K_{vff}

From these transfer functions, $G_{\mathrm{ctrl}}(s)$ is found to be

$$G_{\mathrm{ctrl}}(s) = \frac{V_{\mathrm{carrier,BPCM}}(s) + V_{\mathrm{carrier,out}}(s)}{V_{\mathrm{PWM}}(s)} = \frac{1}{s^2LC + s(L/R_{\mathrm{load}}) + 1} \times \left[K_{\mathrm{cfb}}\frac{N_L}{1+s\tau_{\mathrm{est}}}\frac{sL(sR_{\mathrm{load}}C+1)}{R_{\mathrm{load}}} + K_{\mathrm{vfb}}\right] \quad (29)$$

Obviously, this transfer function cannot be reduced to a simple integrator provided that the poles of the output filter are complex and that $\tau_{\mathrm{est}} < \infty$, thus making the carrier optimization nontrivial as previously stated. With the output filter transfer function $G_{\mathrm{filter}}(s)$ as a factor in $G_{\mathrm{ctrl}}(s)$, it makes sense to start by computing the step response of the output filter transfer function, $G_{\mathrm{filter}}(s)$, given as

$$G_{\mathrm{filter}}(s) = \frac{1}{s^2LC + s(L/R_{\mathrm{load}}) + 1} \quad (30)$$

Assuming R_{load} to be very high (a "high-Q" approximation), this simplifies to

$$G_{\substack{\mathrm{filter}\\ Q>>1}}(s) \approx \frac{1}{s^2LC+1} = \frac{\sqrt{(1/LC)}}{s^2+\sqrt{(1/LC)}} \quad (31)$$

Combining this with the Laplace transform of a step function ($1/s$) results in an expression that can be easily reverse Laplace transformed. The response of the output voltage to a PWM voltage step is hereby found to be

$$V_{\mathrm{out,step}}(t) = \ell^{-1}\left\{\frac{1}{s}\times\frac{\sqrt{(1/LC)}}{s^2+\sqrt{(1/LC)}}\right\} = 1-\cos\left(\frac{1}{\sqrt{LC}}t\right) \quad (32)$$

The output voltage feedback component of the carrier signal thus exhibits the following step response:

$$V_{\mathrm{carrier,out,step}}(t) = K_{\mathrm{vfb}}\left[1-\cos\left(\frac{1}{\sqrt{LC}}t\right)\right] \quad (33)$$

The current estimator output can be usefully reexpressed as

$$V_{\mathrm{carrier,BPCM}}(s) = V_{\mathrm{PWM}}(s)\left[1-G_{\mathrm{filter}}(s)\right]\frac{K_{\mathrm{cfb}}N_L}{1+s\tau_{\mathrm{est}}} \quad (34)$$

Note that at the frequencies of interest for carrier shaping (frequencies in the range around the switching frequency), $G_{\mathrm{filter}}(s)$ is negligible compared to 1 (the filter cutoff can be more than a decade away from the switching frequency), allowing this contribution to be neglected. Practically, this corresponds to assuming the output voltage to be constant, i.e., free from switching ripple. This is also intuitively reasonable since the ac component in the PWM signal will be much larger than the ripple voltage in any practical design. Therefore

$$V_{\mathrm{carrier,BPCM}}(s) \approx V_{\mathrm{PWM}}(s)\,K_{\mathrm{cfb}} \times \frac{N_L}{1+s\tau_{\mathrm{est}}} \quad (35)$$

The response of the BPCM component of the carrier to a PWM step is hereby

$$V_{\mathrm{carrier,BPCM,step}}(t) = \ell^{-1}\left\{\frac{1}{s}\times K_{\mathrm{cfb}}\times\frac{N_L}{1+s\tau_{\mathrm{est}}}\right\} \quad (36)$$

Again, doing a reverse Laplace transformation, this can be reexpressed as

$$V_{\mathrm{carrier,BPCM,step}}(t) = K_{\mathrm{cfb}}\times N_L\times\left[1-e^{-\tau_{\mathrm{est}}t}\right] \quad (37)$$

Hereby, it has been found that the carrier response to a PWM voltage step is approximately

$$V_{\mathrm{carrier,step}}(t) \equiv \mathrm{step}\left\{G_{\mathrm{ctrl}}(s)\right\} \approx K_{\mathrm{vfb}}\left[1-\cos\left(\frac{1}{\sqrt{LC}}t\right)\right] + K_{\mathrm{cfb}}N_L\left[1-e^{-\tau_{\mathrm{est}}t}\right] \quad (38)$$

Now, the carrier signal slope can expressed as

$$\dot{V}_{\mathrm{carrier,step}}(t) = \frac{K_{\mathrm{vfb}}}{\sqrt{LC}}\sin\left(\frac{1}{\sqrt{LC}}t\right) + \frac{K_{\mathrm{cfb}}N_L}{\tau_{\mathrm{est}}}\times e^{-\tau_{\mathrm{est}}t} \quad (39)$$

To ensure that this signal has a constant slope (at least over a brief time horizon following the step), the following optimality criterion is applied as per step 3) in the optimization method:

$$\ddot{V}_{\mathrm{carrier,step}}(0) = 0 \quad (40)$$

Of course, it would be preferable to demand this for all time instances—but this cannot be solved for the BPCM control system since only an integrator has an ideal, constant-sloping step response and $G_{\mathrm{ctrl}}(s)$ of the BPCM amplifier is indeed not an integrator. It should also be noted that this criterion is only useful in a controller structure that is actually capable of producing a triangular carrier signal. This will be the case if the inductor current, or a high-frequency estimate of this is fed back, since the inductor current is (almost) triangular, especially at high switching frequencies. Differentiating the carrier slope leads to

$$\ddot{V}_{\mathrm{carrier,step}}(t) = \frac{K_{\mathrm{vfb}}}{LC}\cos\left(\frac{1}{\sqrt{LC}}t\right) - \frac{K_{\mathrm{cfb}}N_L}{\tau_{\mathrm{est}}^2}\times e^{-\tau_{\mathrm{est}}t} \quad (41)$$

Applying the optimality criterion results in the following simple expression that should be satisfied for an optimal design of the considered BPCM controller:

$$\frac{K_{\mathrm{vfb}}}{LC} = \frac{K_{\mathrm{cfb}}\times N_L}{\tau_{\mathrm{est}}^2} \quad (42)$$

TABLE III
PROTOTYPE BPCM AMPLIFIER DESIGN CONSTANTS

Component	*Value*
L	$20.25\mu H$
C	$2\mu F$
N_L	2:9
τ_{est}	$3.3\mu s$

V. EXAMPLE PROTOTYPE AMPLIFIER DESIGN

To demonstrate the usefulness of the proposed optimization method, a practical amplifier design is considered. Initial design constants are summed up in Table III. The design considered is single-ended and based on the use of 100-V switching components and a 20.25-μH dual-winding power inductor on a gapped RM10 ferrite core, combined with 2 μF of output capacitance. For the typical speaker load of 4–8 Ω, this leads to a minimum filter Q of 1.26, not exactly infinite as approximated, but still underdamped. The current estimator time constant ($\tau_{\rm est}$) was set at 3.3 μs, realized with $R_{\rm est} = 100\ \Omega$ and $C_{\rm est} = 33$ nF.

In order to increase the amplifier immunity to low-frequency supply voltage perturbations, as well as to help establish the carrier voltage dc operating point, the basic BPCM control system is augmented with a parallel integrating control loop as shown in Fig. 14. Equation (42) can still be used to predict the optimum feedback coefficients given that the integrator time constant is kept slow enough compared to the switching frequency, which ensures that the $G_{\rm ctrl}(s)$ step response is not significantly influenced within a time frame of one switching cycle. Note that the paralleling of proportional and integral output voltage feedback effectively provides PI output voltage feedback, hence the term BPCM + PI used for describing this topology. In the implementation shown, the comparator and the operational amplifier run off a single +5 V supply ($V_{\rm cc}$) generated from $+V_s$(34 V.) This is permissible since the operational amplifier has rail-to-rail inputs and the comparator inputs have dc offsets added via resistors to $V_{\rm cc}$.

Taking into account the carrier voltage dc bias resistor $R_{\rm bias}$, the BPCM controller gain constants are given as

$$\begin{aligned} K_{\rm cfb} &= \frac{R_{\rm vfb}||R_{\rm vff}||R_{\rm bias}}{(R_{\rm vfb}||R_{\rm vff}||R_{\rm bias}) + R_{\rm cfb}} \\ K_{\rm vfb} &= \frac{R_{\rm cfb}||R_{\rm vff}||R_{\rm bias}}{(R_{\rm cfb}||R_{\rm vff}||R_{\rm bias}) + R_{\rm vfb}} \\ K_{\rm vff} &= \frac{R_{\rm vfb}||R_{\rm cfb}||R_{\rm bias}}{(R_{\rm vfb}||R_{\rm cfb}||R_{\rm bias}) + R_{\rm vff}} \end{aligned} \tag{43}$$

From these expressions, the ratio $K_{\rm vfb}/K_{\rm cfb}$ can be derived as

$$\frac{K_{\rm vfb}}{K_{\rm cfb}} = \frac{R_{\rm cfb}}{R_{\rm vfb}} \tag{44}$$

Setting $R_{\rm vfb} = 10\ {\rm k}\Omega$, the analytically predicted optimal $R_{\rm cfb}$ is 8.264 kΩ, which was rounded off to 8.2 kΩ in the prototype design. In order to get a closed-loop gain of 20 dB, $R_{\rm vff}$ was set to 1 kΩ. The carrier dc bias point $V_{\rm carrier,bias}$ was set using $R_{\rm bias}$ from the following expression:

$$V_{\rm carrier,bias} = V_{\rm cc} \times \frac{R_{\rm vfb}||R_{\rm cfb}||R_{\rm vff}}{R_{\rm vfb}||R_{\rm cfb}||R_{\rm vff} + R_{\rm bias}} \tag{45}$$

The choice of $R_{\rm bias} = 3.3\ {\rm k}\Omega$ thus lifts the carrier dc operating point to 1 V, to ensure that the carrier stays within the common-mode input range of the comparator. The prototype design gain coefficients are summed up in Table IV along with the true optimum coefficients and two sets of suboptimal coefficients. The suboptimal designs represent the lumped effect of component tolerances that are likely to be significant in the output filter components. Although $K_{\rm cfb}$ is physically determined only by resistors, deviations in L and C require proportional changes in $K_{\rm cfb}$ for optimality to be preserved, so tolerances on L and C can be directly mapped to a tolerance on $K_{\rm cfb}$ as far as carrier distortion is concerned. Practically, the suboptimal designs were implemented by changing $R_{\rm cfb}$ to 10 kΩ and 6.2 kΩ, respectively.

With the prototype design gain coefficients, the carrier signal unity-step response slope is found to be

$$\dot{V}_{\rm carrier,step}\,(0) = \frac{K_{\rm cfb} \times N_L}{\tau_{\rm est}} \approx 5.39\,{\rm mV}/\mu{\rm s} \tag{46}$$

With a nominal supply voltage V_s of 34 V, this means that a 34 V step is applied to $G_{\rm ctrl}(s)$ for $D = 0.5$, leading to a carrier signal slope of 183 mV/μs. This means that the K [23] of the design is

$$K \equiv 2 \times \left.\frac{dV_{\rm carrier}}{dt}\right|_{D=0.5} = 2V_s \times \frac{K_{\rm cfb}N_L}{\tau_{\rm est}} \approx 0.366\,{\rm V}/\mu{\rm s} \tag{47}$$

where K can also be found as follows [23]:

$$K = 2V_s \times {\rm step}\left\{\lim_{s\to\infty} G_{\rm ctrl}(s)\right\} \tag{48}$$

Since the switching frequency of a triangular-carrier hysteretic control system is a parabolic function of duty cycle [16], [33], [35], [37] given quite precisely by

$$f_{\rm sw}\,(D) = \frac{D\,(1-D)}{2(V_{\rm hyst}/K) + t_d} \tag{49}$$

then, for a nominal ($D = 0.5$) switching frequency $f_{\rm sw,nom}$ of 350 kHz, assuming 100 ns comparator/power stage delay t_d, the hysteresis level $V_{\rm hyst}$ should be

$$V_{\rm hyst} = \frac{K}{2}\left[\frac{1}{4f_{\rm sw,nom}} - t_d\right] \approx 110\,{\rm mV} \tag{50}$$

Note that the hysteresis window of the comparator in this case is still defined as $\pm V_{\rm hyst}$. The desired hysteresis window is easily implemented by proper choice of the resistors (R_{h1}–R_{h4}) attached to the noninverting comparator input. The prototype design used $R_{h1} = 33\ {\rm k}\Omega$, $R_{h2} = 3.3\ {\rm k}\Omega$, $R_{h3} = 22\ {\rm k}\Omega$, and $R_{h4} = 3.3\ {\rm k}\Omega$.

VI. SIMULATED/CALCULATED RESULTS

The accuracy of the proposed carrier distortion optimization method and the sensitivity of the optimum to parameter variations were examined by PSpice simulation and the results are

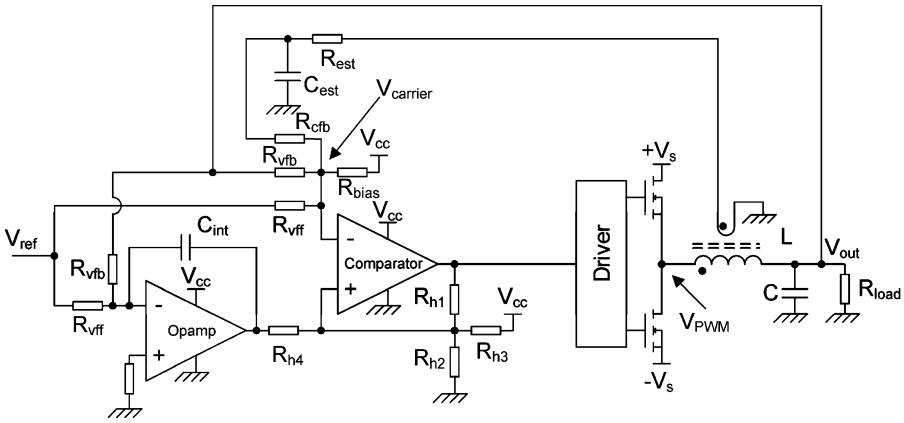

Fig. 14. Hysteretic SO BPCM + PI controlled single-ended amplifier with single-supply ($V_{\rm cc}$) control circuitry.

TABLE IV
OPTIMAL AND IMPLEMENTED BPCM AMPLIFIER DESIGN GAIN COEFFICIENTS

Parameter	Optimal design	Prototype design	Sub-optimal design I ("-20%")	Sub-optimal design II ("+29%")
K_{cfb}	0.0800	0.0800	0.0665 (-20%)	0.103 (+29%)
K_{vfb}	0.0661	0.0656 (-0.7%)	0.0665 (+0.7%)	0.0639 (-3.4%)
K_{vff}	0.661	0.656	0.665	0.639

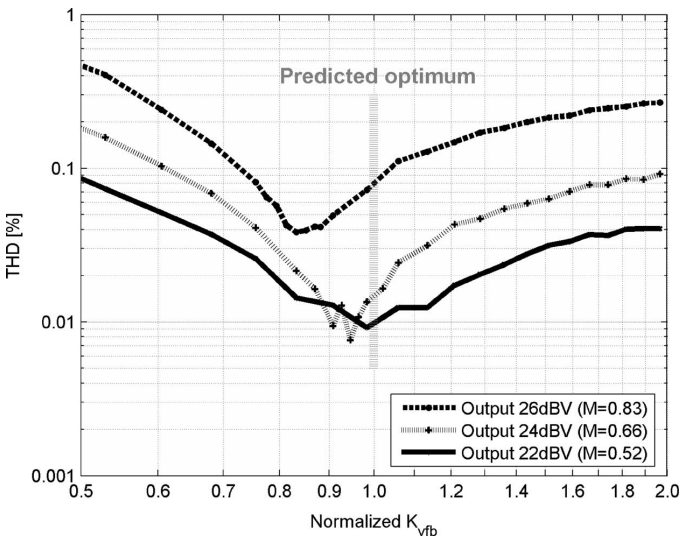

Fig. 15. Simulated THD (3rd + 5th harmonics only) with $K_{\rm vfb}$ values around the predicted optimum.

shown in Fig. 15. A simulation model of the found optimum BPCM + PI design was implemented, with the switching components made ideal so that only carrier distortion was generated. The output THD of the BPCM + PI amplifier simulation model was evaluated for three different amplitudes of 5-kHz sine wave output. In each case, voltage feedback coefficient $K_{\rm vfb}$ was varied from 0.5 to 2 times ($\pm$6 dB) its predicted optimum value. As can be seen, the proposed method succeeds in finding the $K_{\rm vfb}$ that leads to minimal THD for low output levels. The optimal $K_{\rm vfb}$ is seen to vary with output level, however, with a lower $K_{\rm vfb}$ (or a higher $K_{\rm cfb}$) being preferable at high output levels. This suggests that a true global optimum feedback coefficient weighting does not exist and that each output level has its own optimum $K_{\rm cfb}/K_{\rm vfb}$. The amount of carrier distortion generated is seen to be relatively sensitive to component tolerances; optimizing the amplifier for 24 dBV output by choosing a $K_{\rm vfb}$ of 0.95, $\pm$10% $K_{\rm vfb}$ variation is enough to cause a THD increase from 0.01% to 0.02% at 24 dBV output. For $\pm$20%, the THD potentially increases to 0.03%. Still, these numbers are far lower than what would probably be obtained by not paying attention to carrier distortion; for all three output levels, THD varies by a factor of around 10 for relatively modest $K_{\rm vfb}$ variations of $\pm$6 dB around the predicted optimum. An interesting point to note is that even though the amplifier loop gain increases with $K_{\rm vfb}$, overall distortion also increases when $K_{\rm vfb}$ is too high, showing that loop gain maximization alone is not necessarily the best strategy for linearizing SO class-D amplifiers. When combined with minimization of carrier distortion, however, maximized loop gain is still an advantage. This is because 1) high loop gain reduces the amplifier's sensitivity to other disturbances than carrier distortion and 2) loop gain still has an effect on carrier distortion. As seen from (24), designing for a high-gain $G_{\rm ctrl}(s)$ in the audio band directly reduces sensitivity to carrier distortion. There is a complication associated with this, however, since increasing the magnitude of $G_{\rm ctrl}(s)$ also requires an increase in the amount of hysteresis needed for a given switching frequency thereby also increasing the amount of carrier dc variation by the same amount. To maximize loop gain while maintaining carrier distortion, it is therefore necessary to increase the low-frequency magnitude of $G_{\rm ctrl}(s)$ while still ensuring a linear step response and not increasing K as seen from (48) and (49). A difficult exercise, this is at least made somewhat easier by the avail-

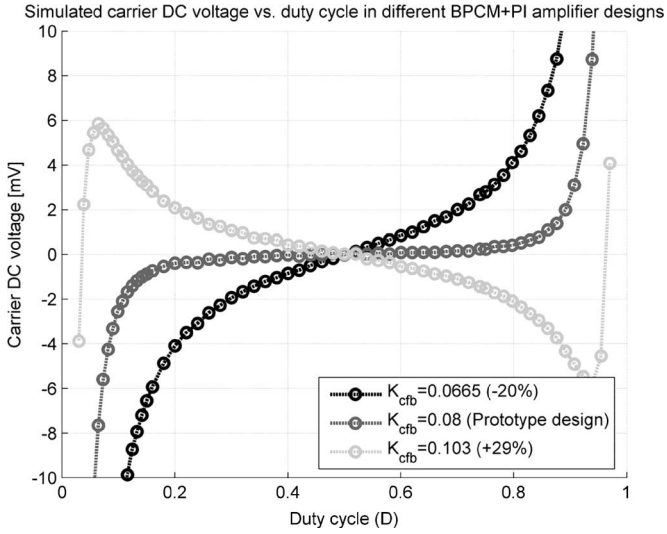

Fig. 16. Simulated carrier dc voltage versus steady-state duty cycle for prototype and suboptimal BPCM + PI amplifier designs. Implemented design can be expected to be very linear for duty cycles from 0.2 to 0.8 (corresponding to an $M < 0.6$ or 23 $\mathrm{dBV_{rms}}$ sine wave from $V_s = 34$ V).

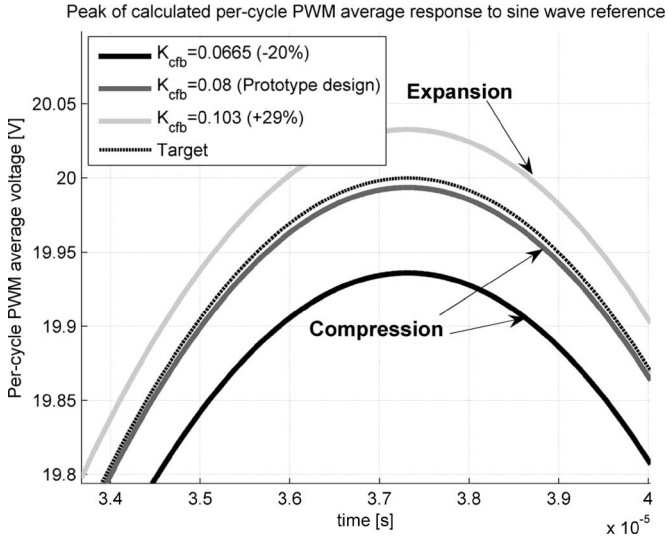

Fig. 17. Calculated sine wave responses of optimal and suboptimal amplifier implementations at 20 V_{peak} (23 $\mathrm{dBV_{rms}}$ or $M = 0.6, D_{\max} = 0.8$) output level. The optimized design is visibly more ideal than the suboptimal designs.

ability of the proposed method for optimizing the $G_{\mathrm{ctrl}}(s)$ step response.

In order to further quantify the carrier distortion mechanism, the methodology already used for THD calculation on the simple AIM controller was adapted for the BPCM + PI system. Due to the complexity of $G_{\mathrm{ctrl}}(s)$ of the BPCM + PI controller, simulation, rather than analysis, was used to determine $V_{\mathrm{carrier,dc}}(D)$. The control loop time delay t_d was set to zero to avoid masking of the nonlinear, dc variation caused by any nonintegrator $G_{\mathrm{ctrl}}(s)$, by the linear, delay-induced variation [21], [35]. The results are shown in Fig. 16 for the nearly-optimal implemented design as well as for the suboptimal designs. It is generally apparent that the relatively slight variation in K_{cfb} causes the carrier average to exhibit significantly more nonlinear variation with duty cycle; hence, the THD can also be expected to increase. As shown in Fig. 17, the generated carrier distortion is expansive (like in the AIM) when the current feedback component is too high since this leads to an overemphasis of the exponential carrier component. Conversely, the carrier distortion instead becomes compressive when the output feedback component is too high.

For THD calculations, the data from Fig. 16 was used (interpolating between data points) to calculate the amplifier response to a sine wave. The sine wave was assumed to have a frequency above the PI corner frequency (i.e., integral output voltage feedback is assumed negligible compared to proportional feedback), allowing (29) to be used for $G_{\mathrm{ctrl}}(s)$, which was then assumed to be flat within the audio band. This is justified by the fact that the inductor current signal is effectively high-pass filtered (see (29)) by the current estimator, so that the output voltage feedback via K_{vfb} dominates at low frequencies. With the low-frequency approximation $G_{\mathrm{ctrl}}(s) = K_{\mathrm{vfb}}$, the method used for the THD calculation in the AIM was applicable. Results for the prototype and suboptimal designs are shown in Fig. 18, where it is confirmed that THD performance is quite sensitive to the carrier composition. For example, inspecting Fig. 18, an amplifier rated for 0.02% maximum THD would have its rated output power reduced by a factor of two (3 dB) with a K_{cfb} tolerance of 20%. As will be demonstrated in the experimental section, this is a reasonable claim since carrier distortion is shown to be the dominant nonlinearity at high output levels. For the optimal design, THD is predicted to stay at a very low level (less than 0.01%) up to 24 $\mathrm{dBV_{rms}}$ output level, where a sharp increase is observed as the carrier average voltage deviates strongly from zero at the peaks of the sine wave.

VII. Experimental Results

The BPCM + PI amplifier in Fig. 14 was implemented on a four-layer printed circuit board (PCB) with one-sided component placement as shown in Fig. 19. Small IRF6645 (28 mΩ, 100 V, 14 nC gate charge) MOSFETs were used together with ample dead time (around 15 ns) to allow cooling via the PCB. A standard HIP2100 with input-side residual current device networks for setting the dead time was used for the MOSFET driver along with a discretely built phase-split/level-shift circuit for interfacing with the LMV7219 comparator.

THD + N measurements were performed using an Audio Precision System 2 with 22 kHz bandwidth without the Aux-25 prefilter. The raw distortion and noise generated by the control system are assessable from the no-load THD + N versus output level measurements in Fig. 20. These measured results are directly comparable to the calculated ones in Fig. 18, since the third and fifth harmonics were found (via the fast fourier transform function) to dominate the generated THD. To ensure a flat $G_{\mathrm{ctrl}}(s)$ as assumed for the calculations in Fig. 18, C_{PI} was temporarily doubled to 100 nF, effectively halving the integral feedback term. The measurements confirm

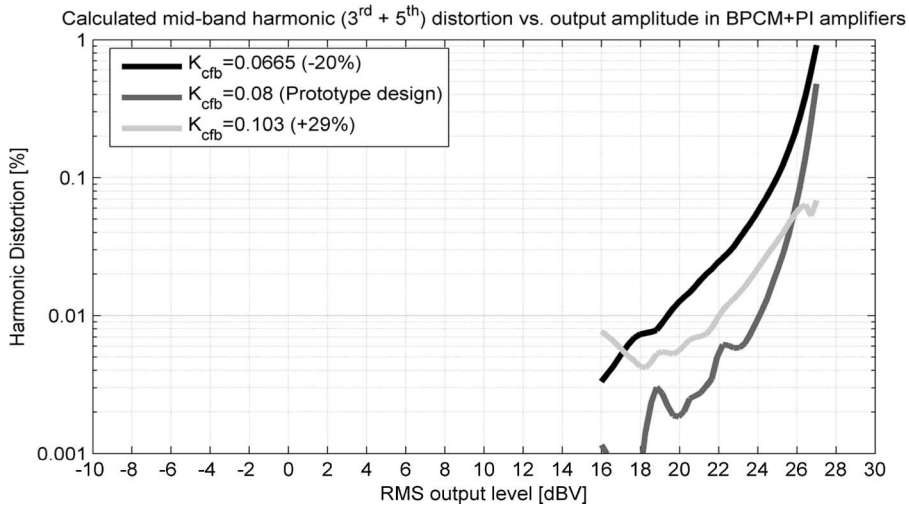

Fig. 18. Calculated THD (3rd + 5th harmonics only) caused by carrier distortion in optimum and implemented prototype BPCM + PI amplifier designs with variable $K_{\rm cfb}$. For the implemented design, no-load THD is expected to be less than 0.02% below 25 $\rm dBV_{rms}$ ($M = 0.74$ or $D_{\max} = 0.87$ output level.

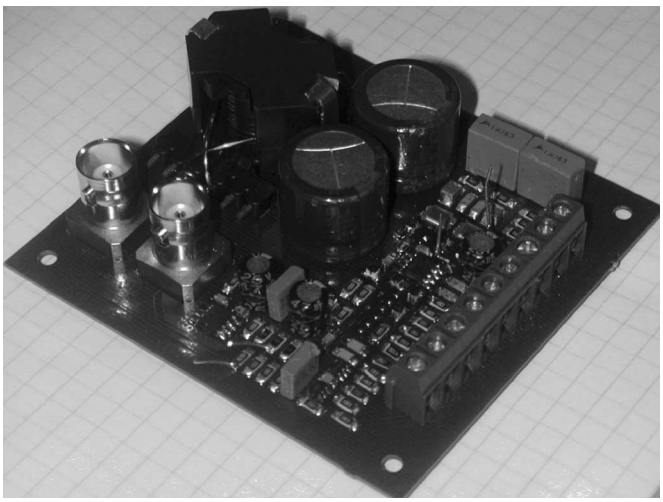

Fig. 19. Prototype hysteretic BPCM + PI amplifier PCB.

that even modest – 20% or +29% deviation from the optimal carrier composition creates significant THD at high output levels. Some deviation is evident below 25 dBV (particularly in the "+29%" implementation), but agreement is very good above this level.

Given that the optimized prototype design produces higher THD at high levels than the "+29%" design, it is of course debatable whether or not it is in fact optimal. However, by defining the optimal design as the one that provides the lowest THD at low output levels, optimality has been achieved. As also predicted by simulations in Fig. 15, linearity can be increased at high output levels by increasing $K_{\rm cfb}$ (or lowering $K_{\rm vfb}$) thereby sacrificing low-level performance Such tradeoffs are best implemented following a precise specification of the desired THD and output power performance of the amplifier.

The noise generated by the BPCM + PI amplifier is 240 μV since THD + N is 0.02% at 0 $\rm dBV_{rms}$ output level where noise is dominant (as seen by the 6 dB/octave slope of the THD + N curve). This is a rather high number that could probably be reduced by the use of a slower comparator. This is because [29] the comparator integrates the circuit noise (generated by resistors and active components) during the time when the switching decision is made, and slower comparators have a longer decision "window," effectively averaging the applied noise for a longer period.

The triangularity of the carrier signal in the three different configurations is assessable from the measurements in Fig. 21. Visually, the optimized carrier signal appears the most triangular, as also expected for the design with the lowest THD.

The performance of the implemented power switching stage was examined using the "analog persist" function on a Lecroy WaveRunner oscilloscope. This allowed observation of the total spread in variation of the switch node behavior with load current. For a sinusoidal output current of ±6.25A, a 15 ns spread in transition delay time was observed as seen in Fig. 22. This is a result of the use of 15 ns dead time and a ripple current of 2.4 $\rm A_{pp}$, leading to the power stage operating in both the zero current switching (ZCS) mode (for output currents less than ±1.2A, given enough dead time) and hard-switched mode (for higher output currents).

The THD + N performance of the prototype design with the usual 4 Ω and 8 Ω loads and three commonly used test frequencies (100 Hz, 1 kHz and 6.7 kHz) is indicated in the measurements in Figs. 23 and 24. The maximum frequency of 6.7 kHz is often used for switch-mode amplifiers since the third harmonic distortion of higher frequencies falls outside of the commonly used 20–22 kHz measurement bandwidths. Due to the dominance of the integral voltage feedback term at low frequencies, the 100 Hz THD figures are very low. The use of higher-order integral low-frequency feedback allows extremely low THD to be obtained at low frequencies [5], [6], [9], but usually does not help at higher frequencies since the loop gain inevitably has to roll off. Additionally, it is obvious that taking extra integral feedback too far will result in an increase in carrier

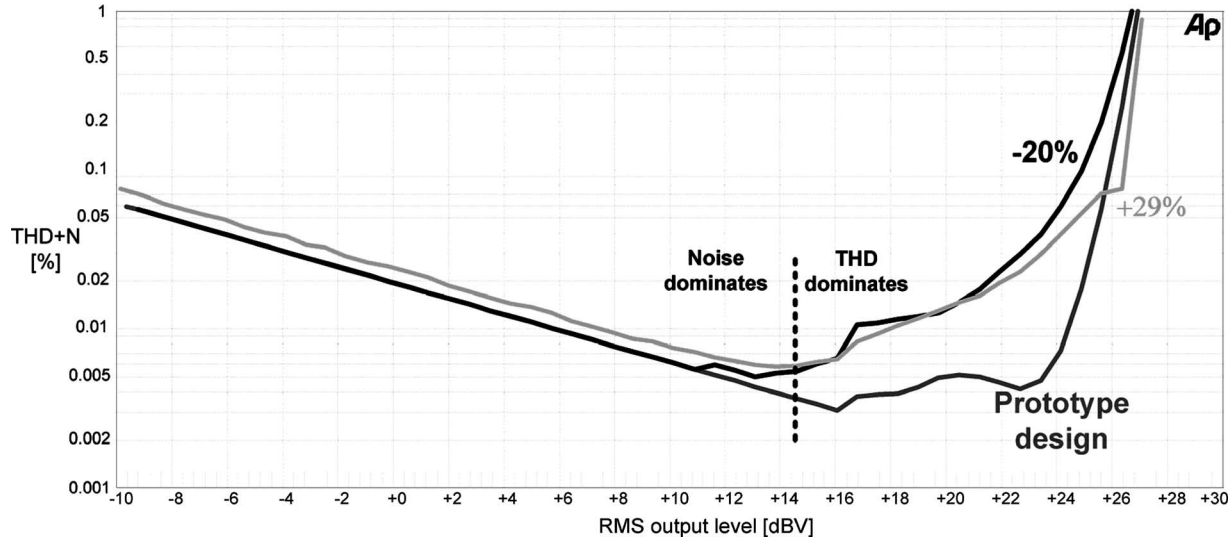

Fig. 20. Unloaded prototype amplifier THD + N versus output level ($0\ \mathrm{dBV} = 1\ V_{\mathrm{rms}}$) at 1 kHz with optimal and suboptimal K_{cfb}, for comparison with Fig. 18. THD of the optimized design is less than 0.02% up to 25 $\mathrm{dBV_{rms}}$. Suboptimal designs have higher THD as expected.

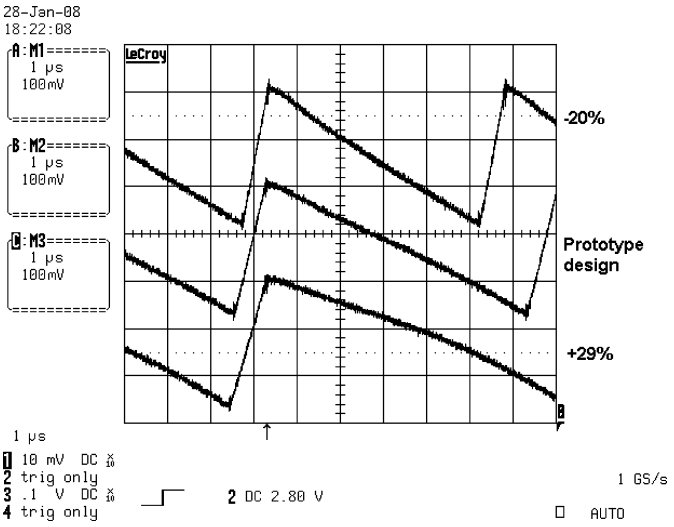

Fig. 21. Prototype carrier waveforms for $D = 0.88$ (peak of $M = 0.76$ sine wave.) Optimized design runs at 150 kHz, indicating an idle switching frequency of 350 kHz. The optimized carrier visually appears to be the most triangular, as also targeted by the proposed optimization method.

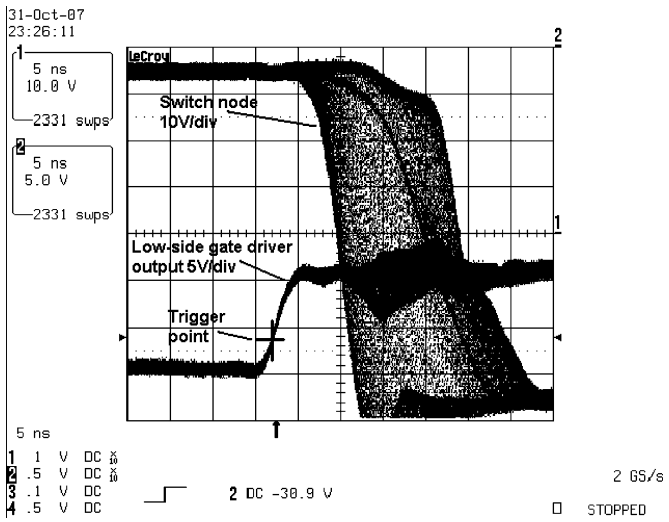

Fig. 22. Variation of switching behavior of prototype, measured using the "analog persist" function. Output is an 80 W ($25\ V_{\mathrm{peak}}$) sine wave into 4 Ω and there is evidently a switching transition point variation of around 15 ns due to the combination of dead time and variation in load current.

distortion, since a higher-than-first-order integral of a PWM signal is not triangular.

Overall, the presented design can be rated at 80/45 W with less than 0.03% THD + N for 4/8 Ω, which is a very decent result for a design done purely by analysis. As indicated by Fig. 20 and the analysis performed, it would in fact be quite difficult to come up with a significantly better design given the BPCM feedback topology and the power stage used. This statement is backed up by results from prior art, which are summarized in Table V. Control schemes, power stage configurations, and switching frequencies are also listed for reference. BTL refers to "Bridge Tied Load," i.e., the full-bridge configuration while SE refers to "single-ended." Other very noteworthy results exist [6], [11], but details are inadequate for comparative purposes. It should of course be noted that the power stage components used in the presented paper are nearly state of the art with discrete components and that this of course impacts the results positively. However, it was shown in Figs. 18 and 20 that carrier distortion generates exactly 0.02–0.03% THD for $M = 0.75$, so it is the carrier distortion that dictates the final THD specification of the design. Hence, the presented optimization method has been shown to be instrumental in obtaining the THD results in Figs. 23 and 24. This was indeed also the conclusion in [5] for the discrete-time-based optimization method for fixed-frequency PWM-based amplifiers. It is expected by the authors that future publications will demonstrate a clear link between the proposed averaging and time-domain-based view of "carrier distortion" and the discrete-time and frequency-domain-based view of "aliasing distortion" [5]. The presented averaging approach is principally also applicable for THD prediction in phase-shift

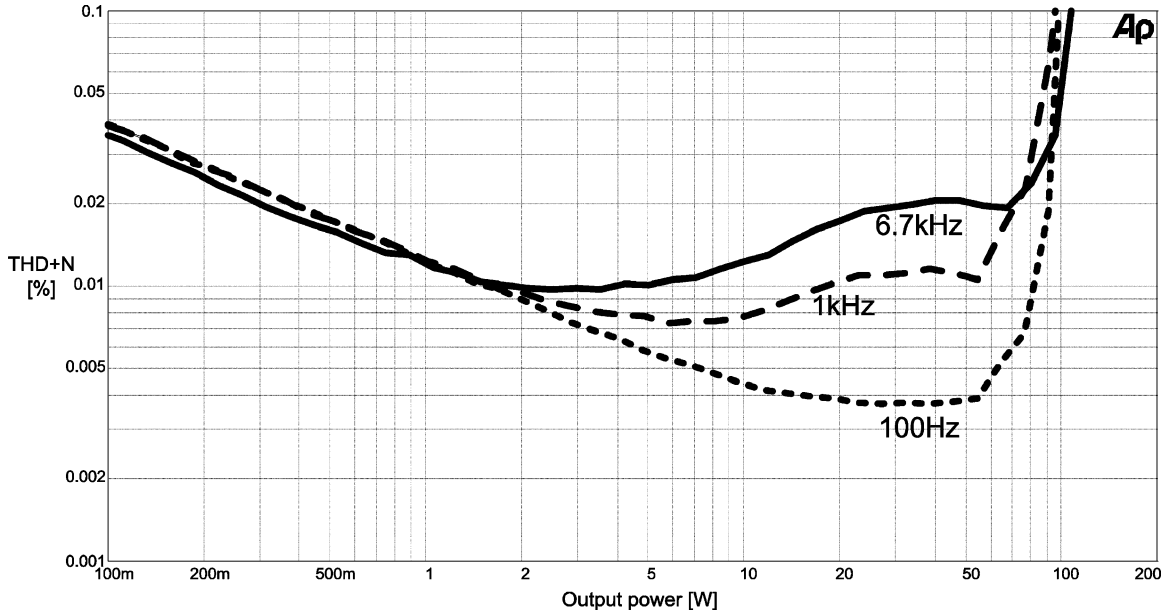

Fig. 23. Optimized prototype amplifier THD + N versus output power with a 4 Ω load. Worst case (below 80 W or $M = 0.75$) THD + N is very respectable at 0.03% at 6.7 kHz.

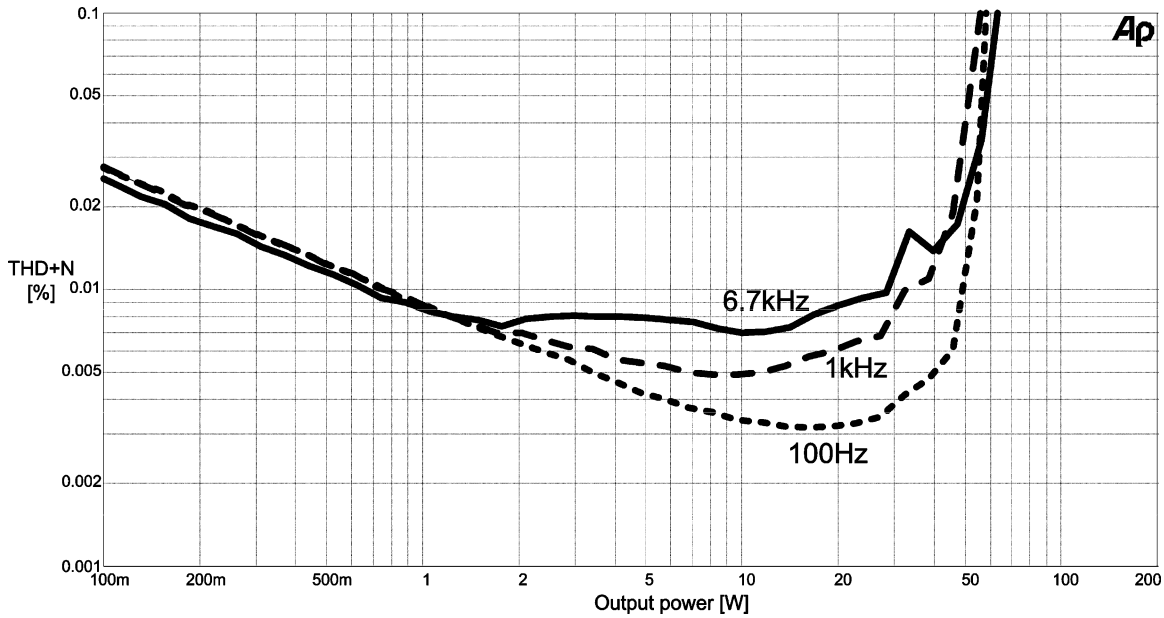

Fig. 24. Optimized prototype amplifier THD + N versus output power with an 8 Ω load. Distortion stays below 0.02% below 45 W, corresponding to $M = 0.79$.

SO control systems [6]–[8], where the carrier signal is sinusoidal and oscillation is induced by raw phase shift in the loop filter $G_{\mathrm{ctrl}}(s)$ rather than by comparator hysteresis. The carrier average in these systems will also potentially exhibit nonlinear variation with duty cycle. However, averaging the carrier signal in such systems is nontrivial since oscillation is only possible if the loop filters are second-order or higher [7] or comparator time delay is added to the analysis.

Finally, one important amplifier parameter that has not yet been considered, namely the frequency response, is examined in Fig. 25. For the typical 4–8 Ω load, the frequency response is fortunately flat within 1.2 dB below 20 kHz. Prefiltering could be used to straighten this out if desired. Computation of the frequency response for verification is easily done using the classical sliding mode approximation, but falls outside the scope of this paper.

TABLE V
REPRESENTATIVE PRIOR ART THD + N RESULTS FOR COMPARISON WITH PRESENTED STUDY

Reference	THD+N, 4Ω, M=0.75, 6.7kHz	THD+N, 8Ω, M=0.75, 6.7kHz	Control topology	Power stage, supply voltage, f_{sw}
[5]	?	0.018%	Fixed-freq. PWM + "MAE filter"	BTL, 55V, 350kHz
[9]	0.04%	?	Hysteretic SO, "GLIM"	SE, +/-40V, 350kHz
[38]	?	0.05%	One-cycle	BTL, 54V, 250kHz
This work	0.03%	0.02%	Hysteretic SO, BPCM+PI	SE, +/-34V, 350kHz

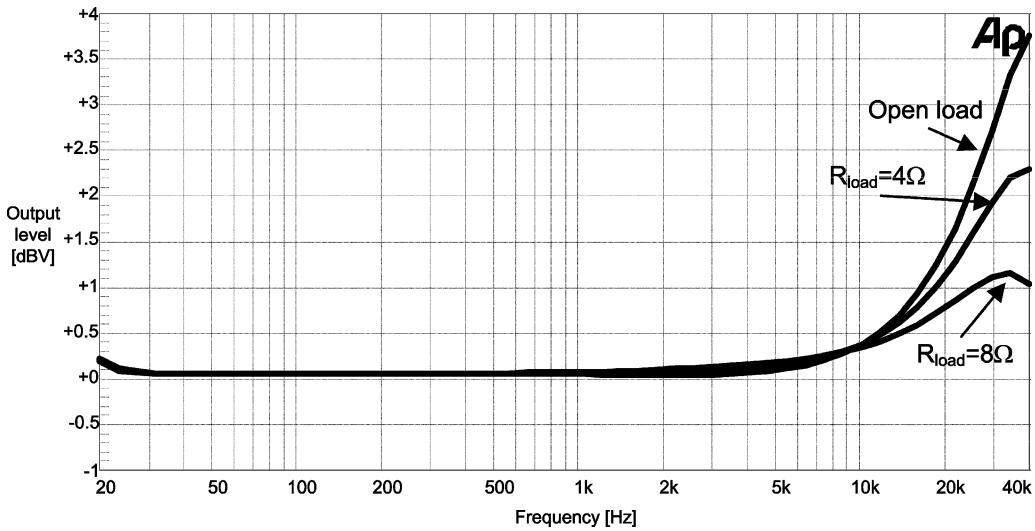

Fig. 25. Measured frequency responses of prototype amplifier. With a typical speaker load (4–8 Ω), response is flat within 1.2 dB over the audio band (20 Hz to 20 kHz.).

VIII. CONCLUSION

An approach for understanding, evaluating, and minimizing the intrinsic distortion generated by hysteretic SO controllers applied to buck-type power converters has been presented. The term "carrier distortion" has been used for this intrinsic distortion phenomenon, referring to prior art. Carrier distortion is mainly an issue of concern in switch-mode ac power amplifiers where the signal bandwidth is high compared to the switching frequency and where fast, high-quality switching components are used. In such cases, distortion generated by imperfect switching is low while loop gain of the control system is limited at high signal frequencies, making carrier distortion the dominant nonlinearity in the power amplifier at high output levels. Class-D audio power amplifiers are an obvious application for the presented analysis, but reducing harmonic distortion of switch-mode power amplifiers is also of interest in a variety of other niche applications. Examples include xDSL drivers, envelope-tracking power supplies, and ac transmission line filters.

In agreement with prior art statements, it has been found that the carrier signal (a.k.a. sliding variable) should be made triangular by proper design of the control loop(s) to minimize this distortion. This directly resulted from an averaging analysis of the steady-state hysteretic comparator input/output waveforms. It was shown that even an amplifier with a perfect power stage supplied with a perfect dc supply voltage can in fact produce significant harmonic distortion due to the carrier distortion mechanism. Based on the desire for a triangular carrier signal for minimizing carrier distortion, a simple s-domain analytical approach was proposed and demonstrated on a nontrivial control topology. An optimized prototype amplifier design was implemented and verified against modeled results. The generated harmonic distortion was found to be well described by the proposed methodology as well as quite sensitive to parameter variation. The harmonic distortion results achieved with the prototype design were at state-of-the-art level, verifying the validity and usefulness of the presented approach.

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